Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Withdrawn) A reticle for use in a lithographic process, comprising:

a patterned layer located over a reticle substrate; and

a test pattern located over said reticle substrate, wherein a portion of said test pattern is within a step-distance of a portion of said patterned layer, a variance in said test pattern being indicative of a variance in said patterned layer.

2. (Withdrawn) The reticle as recited in Claim 1 wherein said portion of said test pattern is a first portion of said test pattern and said potion of said patterned layer is a first portion of said patterned layer and wherein said first portion of said test pattern is within a step-distance of said first portion of said patterned layer and a second portion of said test pattern is within a step-distance of a second portion of said patterned layer, a variance between said first and second portions of said test pattern being indicative of a variance between said first and second portions of said patterned layer.

3. (Withdrawn) The reticle as recited in Claim 1 wherein said test pattern includes a reoccurring line/space structure.

4. (Withdrawn) The reticle as recited in Claim 3 wherein said line/space structure has a pitch of less than about 3/2 the wavelength in use.

5. (Withdrawn) The reticle as recited in Claim 1 wherein said test pattern has a length greater than said step-distance.

6. (Withdrawn) The reticle as recited in Claim 1 wherein said test pattern is located inside a pellicle frame of said reticle.

7. (Withdrawn) The reticle as recited in Claim 1 wherein said test pattern is located in a scribe region defined by said patterned layer.

8. (Withdrawn) The reticle as recited in Claim 1 wherein said variance is a systematic variance in critical dimension (CD) in said patterned layer.

9. (Currently amended) A method for monitoring critical dimension (CD) variations of a reticle, comprising:

providing a reticle layer over a reticle substrate, said reticle layer including each of:

a patterned feature area corresponding to a desired circuitry pattern; and

a test pattern area, wherein a portion of said test pattern area is within a step-distance of a portion of said patterned feature area;

patterning a resist material by stepping said reticle, the patterning including each of the patterned feature area and test pattern area incorporated in said reticle layer; ~~and~~

visually inspecting said resist material for light and dark regions within said test pattern area, said light and dark regions representing a corresponding variance in said patterned feature area of the resist material.

using said resist material as patterned by said reticle to form the feature of a semiconductor device after said visually inspecting.

10. (Previously Presented) The method as recited in Claim 9 wherein said portion of said test pattern area is a first portion of said test pattern area and said portion of said patterned feature area is a first portion of said patterned area and wherein said first portion of said test pattern area is within a step-distance of said first portion of said patterned feature area and a second portion of said test pattern area is within a step-distance of a second portion of said patterned feature area, a variance between said first and second portions of said test pattern area being indicative of a variance between said first and second portions of said patterned feature area.

11. (Previously Presented) The method as recited in Claim 9 wherein said test pattern area creates a reflective grating in said patterned resist material, and said reflective grating is configured to provide said light and dark regions if said variance in said patterned feature area exists.

12. (Original) The method as recited in Claim 11 wherein said reflective grating includes a reoccurring line/space structure.

13. (Currently amended) The method as recited in Claim 12 wherein said reoccurring line/space structure has a pitch of less than about 3/2 ~~the~~ a wavelength ~~in use~~used in said patterning step.

14. (Previously Presented) The method as recited in Claim 9 wherein said test pattern area is located in a scribe region defined by said patterned feature area.

15. (Previously Presented) The method as recited in Claim 9 wherein said variance is a systematic variance in critical dimension (CD) in said patterned feature area.

16. (Original) The method as recited in Claim 9 wherein visually inspecting said material includes visually inspecting said material using an optical microscope.

17. (Original) The method as recited in Claim 16, further including changing a focus on said optical microscope to cause said light and dark regions to become more or less pronounced.

18. (Previously Presented) A method for making a semiconductor device, comprising:

patterning a resist material by stepping a reticle, wherein said reticle includes each of:

a patterned feature area corresponding to a desired feature of a semiconductor device; and

a test pattern area, wherein a portion of said test pattern area is within a step-distance of a portion of said patterned feature area; and

visually inspecting said patterned resist material for light and dark regions within a corresponding test pattern area, said light and dark regions representing a systematic variance in critical dimension (CD) in said patterned resist material;

using said patterned resist material to form the feature of a semiconductor device after said visually inspecting.

19. (Canceled).

20. (Original) The method as recited in Claim 18 wherein said patterned resist material is used to form multiple features, and wherein said multiple features are electrically contacted to form an operational integrated circuit.